Radiation Tolerant Enhancement-Mode Gallium Nitride FETs for High Frequency DC-DC Conversion

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Abstract: *Enhancement-mode GaN-on-Si (eGaN®) FETs have shown superior performance compared to standard MOSFETs. We have demonstrated their ability to operate reliably under harsh environmental conditions and high radiation conditions. GaN-on-Si eGaN FETs have been tested in collaboration with Microsemi product engineers and Microsemi is developing a portfolio of space-level MiGan™ products for use in radiation applications. In this paper we present results characterizing a newly released family of enhancement-mode GaN HEMT transistors designed for higher frequency operation. The stability of these devices under radiation exposure as well as their capability in high-performance DC-DC converters operating at 10 MHz will be presented.*

Keywords:
Gallium Nitride, GaN, eGaN®, MiGan™, MOSFET, FET, Radiation tolerance, SEE, Gamma radiation, buck converter, DC-DC converter.

Introduction:

Enhancement-mode gallium nitride transistors have been commercially available for over four years. In that time they have enabled significant efficiency improvement in commercial DC-DC converters in a variety of topologies and at a variety of power levels [1]. Enhancement-mode transistors from Efficient Power Conversion Corporation (eGaN FETs) used in Microsemi MiGan™ FETs have also been demonstrated to have remarkable tolerance to gamma radiation [2] and single event effects (SEE) [3]. As this is a relatively new technology, advances in product capability are relatively frequent. In September 2013, a new generation of eGaN FETs was introduced that was designed for high power density, multi-megahertz DC-DC conversion. In this paper we present new results characterizing the stability of these devices under radiation exposure and quantify their capability in high-performance DC-DC converters operating at frequencies as high as 10 MHz.

3rd-generation GaN-on-silicon power transistors:

Learning from four years' experience with first- and second-generation eGaN FETs, EPC introduced a third generation family in September 2013. All of the initial members of this family are supplied for commercial use in the wafer level chipscale package (WLSCP) outline shown in Figure 1, and in hermetic packaging by Microsemi Corp. Their key electrical characteristics of the product in hermetic packaging are listed in Table 1.

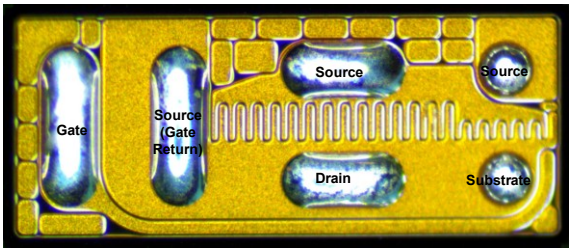

Figure 1: The EPC8000 series WLCSP die showing bump side with pin-out locations.

Table 1: Key electrical characteristics of the MGN8900 family of MiGan™ FETs.

Part Number	BV (V)	$R_{DS(on)}$ MAX (mΩ) (V_{GS} = 5 V, I_D = 0.5 A)	Peak I_D Min (A) (Pulsed, 25°C, T_{PULSE} = 300 µs)	Typical Charge (pC)					R_G Typ (Ω)
				Q_G	Q_{GD}	Q_{GS}	Q_{OSS}	Q_{RR}	
MGN8904	40	125	7.5	358	31	110	493	0	0.4
MGN8907	40	160	6	302	25	97	406	0	0.4
MGN8906	40	250	3.8	211	15	75	264	0	0.4
MGN8908	40	325	2.9	177	12	67	211	0	0.4
MGN8909	65	138	7.5	380	36	116	769	0	0.4
MGN8905	65	275	3.8	218	18	77	414	0	0.4
MGN8902	65	530	2	141	9.4	59	244	0	0.4
MGN8903	100	300	4	315	34	87	1100	0	0.4

Six areas of improvement were implemented in the third generation eGaN FETs.

1. *Separate gate return (source) connection*. The separate source connection for the gate circuit limits the common source inductance to inside the device itself. This reduction in common-source inductance is critical to high frequency performance. The efficiency impact of the common source reduction is well documented [4, 5], and designers can thus focus all their attention on reducing the loop inductance [5].
2. *Low inductance gate connection.* The wider solder bar for the gate circuit connection significantly reduces the inductance of this connection to the gate circuit, thereby enhancing the speed of the connection to the gate driver.
3. *High dv/dt immunity*. An important metric for dv/dt immunity is the Miller ratio, which is an indicator of how susceptible gates are to turning back on at high dv/dt. For the ultra-fast MGN8900 family of devices the Miller ratio (Q_{GD}/Q_{GS1}) has been reduced to below 0.38, well below the industry standard of 1.
4. *Orthogonal gate and drain circuit connections*. The gate and drain solder bars are designed so that optimal connection current paths are 90° with respect to each other. This significantly reduces the inter-action of the gate circuit current with the drain circuit current, and effectively reduces the common source inductance (CSI) of the device.
5. *Low internal parasitic Inductances*. The internal connection routing has been designed with high frequency applications in mind, and therefore internal parasitic inductances have been minimized for both the drain and gate circuits.
6. *Reduced Q_{GD}*. This family of MiGan™ FETs is targeted for lower current applications, and to maximize performance the Miller charge has been reduced, improving switching performance by decreasing the voltage transition times. This comes at a slight increase in Q_{GS2} and di/dt losses, but overall total switching losses are still closely matched.

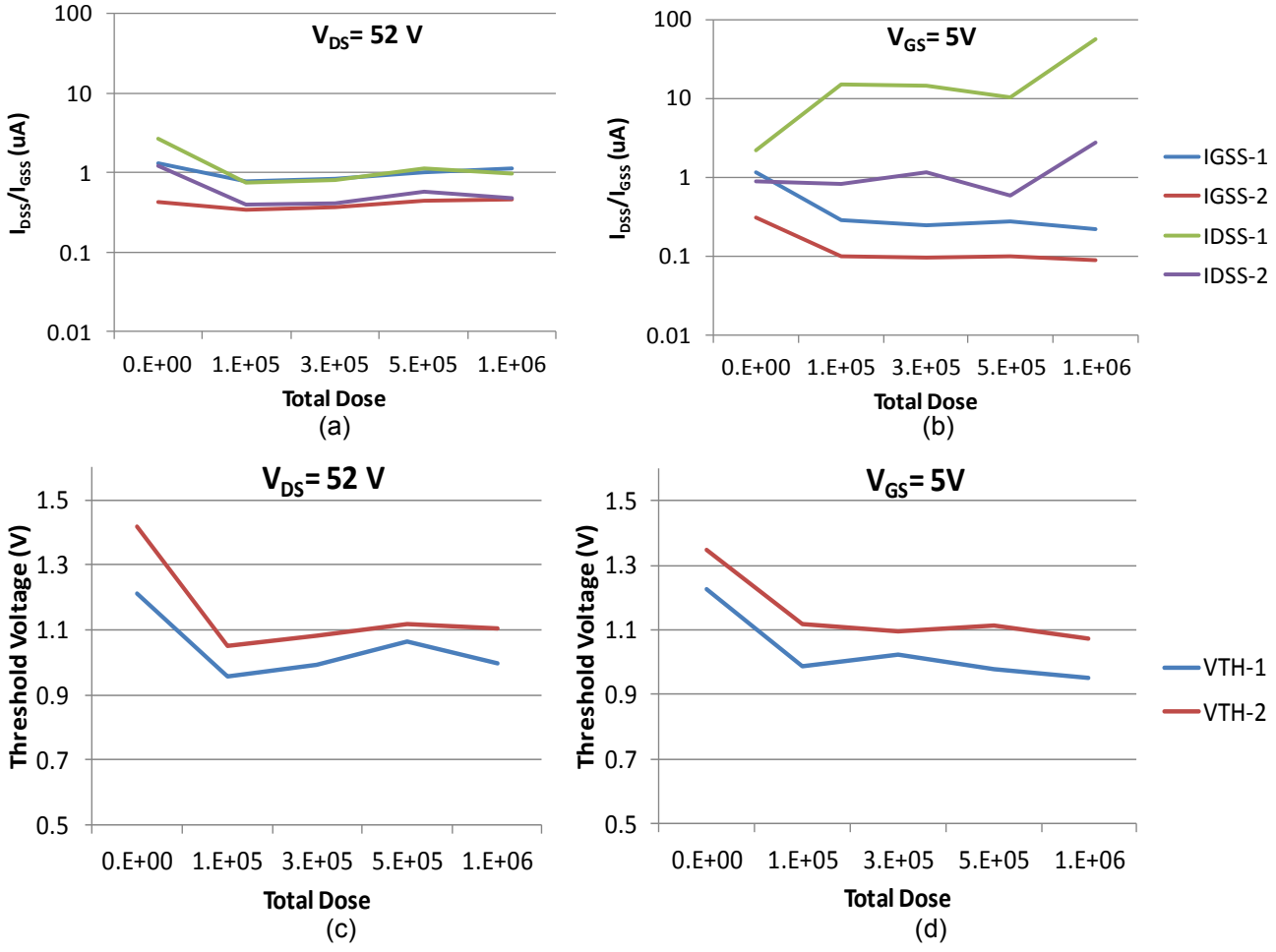

Figure 2: Device parameters for two MGN8909 MiGan™ FETs before and after 1 MRad(Si) total dose exposure; (a) I_{DSS} and I_{GSS} leakage current for total incident dose (TID) testing at 52 V_{DS}, (b) I_{DSS} and I_{GSS} leakage current for TID testing at 5 V_{GS}, (c) Threshold voltage for TID testing at 52 V_{DS}, and (d) Threshold voltage for TID testing at 5 V_{GS}

Total Dose Testing:

Utilizing the "Gamma Cave" at the University of Massachusetts, Lowell, MGN8909 (65 V, 138 mΩ) transistors were subjected to a total gamma dose of 1 MRads (Si) at a dose rate of 96 Rads (Si)/sec. A ^{60}Co source was used and all testing was according to MIL-STD-750, Method 1019. Two different test conditions were used. The first test condition biased the drain-source at 80% of rated $V_{DS(MAX)}$ (52 V in the case of the MGN8909). The second test condition biased the gate-source at 5 V. Examples of the test results are shown in figure 2. All parameters remained well within data sheet limits. Additional testing was performed on third-generation MiGan™ FETs with ratings up to 100 V with generally the same behavior, indicating that these new devices can be used up to at least 1 MRads (Si) without significant performance degradation.

Single Event Effects (SEE) Testing:

SEE Testing is used to quantify the effects of ionizing radiation on electronic devices. Heavy-ion testing of third-generation MiGan™ FETs was performed at the Texas A&M cyclotron following MIL-STD-750E, METHOD 1080 using Au at a linear energy transfer (LET) of 85.4. The results showed that third-generation MiGan™ FETs had a significantly higher level of SEE tolerance compared with power MOSFETs specially designed for this exposure.

With Au as the projectile, no catastrophic failures were created up to full rated voltage for the two types of devices tested. Figure 3 shows the I_{DSS} and I_{GSS} of a representative MGN8909 MiGan™ FET during a series of Au ion exposures at 85.4 LET with a final dosage of $1 \cdot 10^6$ Au/cm^2. The device was biased with 65 V_{DSS} (maximum data sheet rating) and 0 V_{GS}. No significant change in either I_{DSS} or I_{GSS} occurred.

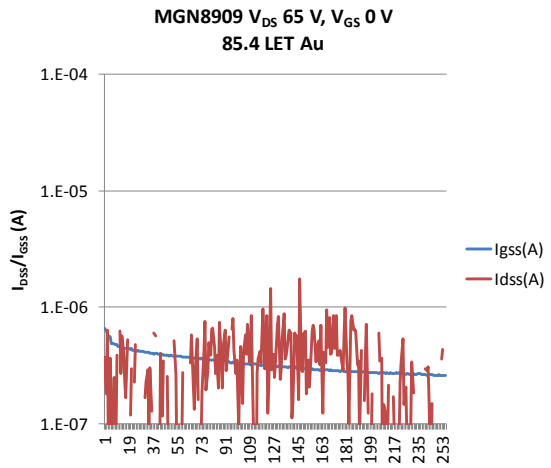

Figure 3: I_{DSS} and I_{GSS} progression for MGN8909 MiGan™ FET during single event testing with $1 \cdot 10^6$ ions/cm^2 Au at 85.4 LET and biased at 65 V_{DSS}.

A similar result was obtained for the cohort of MGN8903 MiGan™ FETs. These parts have a maximum BV_{DSS} rating of 100 V and did not show measurable degradation at 85.4 LET up to the end of the testing at a final dosage of $1 \cdot 10^6$ Au/cm^2 as shown for a typical device in figure 4.

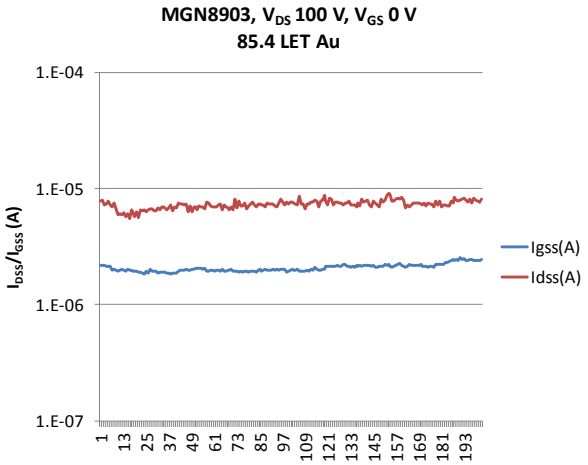

Figure 4: I_{DSS} and I_{GSS} progression for MGN8903 MiGan™ FET during single event testing up to $1 \cdot 10^6$ ions/cm^2 Au at 85.4 LET and biased at 100 V_{DSS}.

Design Example: 10 MHz DC-DC Buck Converter

To show the improved electrical performance of the third-generation family of MiGan™ FETs, a high frequency buck converter was designed. In this example, the EPC8005, the commercial version of the MGN8905, was used in a 42 V_{IN} to 20 V_{OUT}, 20 W buck converter operating at 10 MHz. The basic power circuit is shown in figure 5 where L_{Buck} = 2.2 µH and C_{out} = 2 x 4.7 µF. The main supply (V_{DD}) bus caps were 100 nF. The board was designed using the optimal layout technique [5] to ensure the highest efficiency.

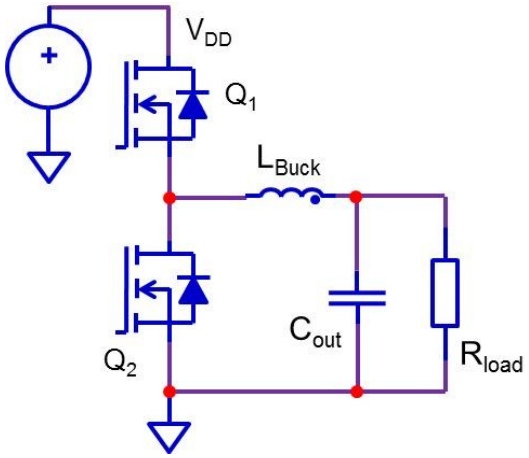

Figure 5: Buck converter schematic.

Figure 6 shows a photo of the evaluation board fitted with EPC8005 transistors and the Texas Instruments' LM5113 gate driver IC. The right image shows the details of the power circuit with the gate driver IC. To maintain low inductance in the gate circuit, two parallel-connected size 0201 resistors were used side by side for the gate resistors, as well as keeping the gate driver IC very close to the devices.

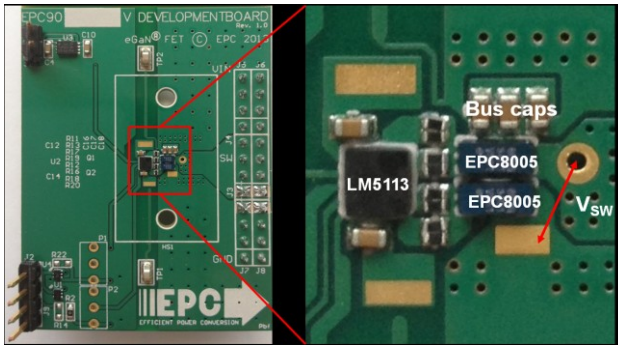

Figure 6: Photo of the evaluation board showing the EPC8005 devices (commercial version of MGN8905) and LM5113 gate driver.

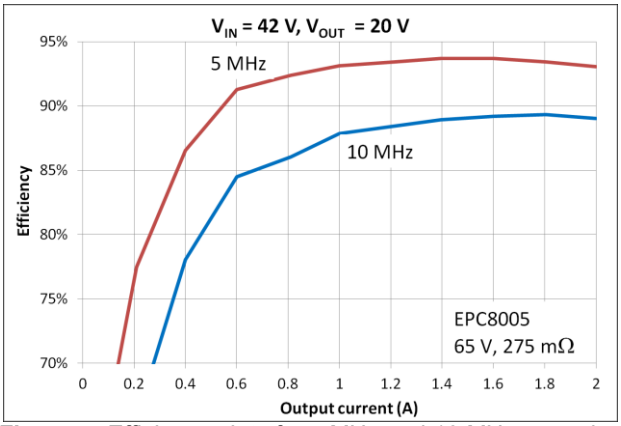

Figure 7: Efficiency plots for 5 MHz and 10 MHz operation of the buck converter.

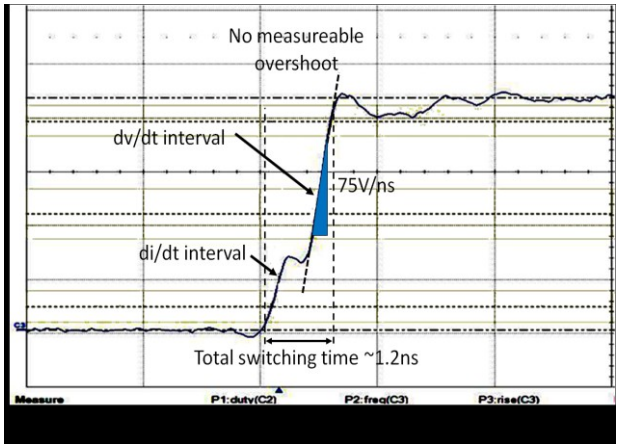

Figure 8: Switch-node voltage waveform for the buck converter.

The converter was tested at both 10 MHz and 5 MHz operation, and the efficiency is given in figure 7. The plots show a respectable 89% peak efficiency while operating at 10 MHz and 94% while operating at 5 MHz. The inductor used in the 5 MHz operation is the same as in the 10 MHz operation, and selecting a more optimal inductance can lead to further improvement. Figure 8 shows the rising edge switch node voltage waveform with V_{in} = 42V, I_{out} = 2A. The total switching time is around 1.2 ns and both the di/dt and dv/dt events can be distinguished. Also of note is the minimal voltage overshoot at completion of the transition.

Summary:

The new third-generation MiGan™ FETs, like their first and second-generation predecessors, show high radiation tolerance in both SEE and gamma dose testing. These GaN-on-silicon power transistors, designed for multi-megahertz switching converter applications, allow the designer of radiation tolerant systems to achieve power densities and efficiencies that equal the commercial state-of-the-art.

References

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